SPECIFICATIONS

PXIe-5164

1 GS/s, 14-bit Reconfigurable Oscilloscope

Contents

NATIONAL INSTRUMENTS

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are *Warranted* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limit filters
- Sample rate set to 1 GS/s
- Onboard Sample Clock locked to onboard Reference Clock
- Calibration IP is used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the *NI Reconfigurable Oscilloscopes Help* for more information about the calibration API.

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C
- The PXIe-5164 is warmed up for 15 minutes at ambient temperature
- Calibration cycle is maintained
- The PXI Express chassis fan speed is set to HIGH, the foam fan filters are removed if present, and the empty slots contain PXI chassis slot blockers and filler panels. For more

information about cooling, refer to the *Maintain Forced-Air Cooling Note to Users* available at *ni.com/manuals*.

- External calibration performed at 23 °C ± 3 °C

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C with a 90% confidence level

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ± 1.25%, typical 1 MΩ ± 0.5%, typical
Input capacitance (1 MΩ)	20.2 pF ± 2.5 pF
Input coupling	AC, DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR), Nominal

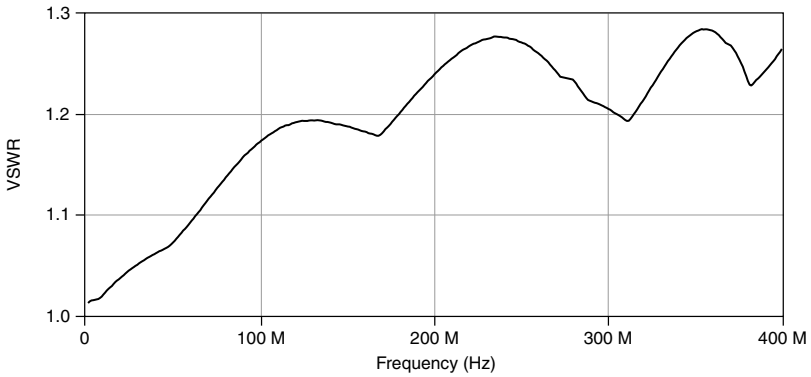
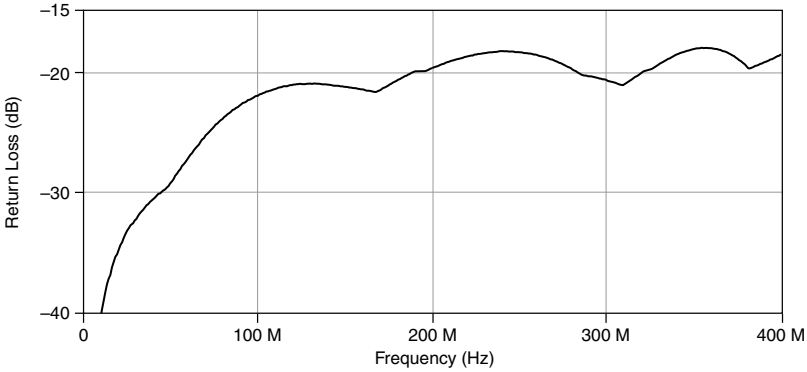


Figure 2. 50 Ω Input Return Loss, Nominal



Voltage Levels

50 Ω FS Input Range (V_{pk-pk})	0.25 V
	0.5 V
	1 V
	2.5 V
	5 V

Table 1. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range (V)[1]
0.25 V	±5
0.5 V	±5
1 V	±5
2.5 V	±10 or ±248.75
5 V	±10 or ±247.5
10 V	±10 or ±245
25 V	±50 or ±237.5

[1] For input ranges between 2.5 V_{pk-pk} and 100 V_{pk-pk}, two offset ranges are possible. The driver software automatically picks the offset range that provides the highest resolution and accuracy.

Table 1. 1 MΩ FS Input Range and Vertical Offset Range (Continued)

Input Range (V_{pk-pk})	Vertical Offset Range (V)[1]
50 V	±50 or ±225
100 V	±50 or ±200

Maximum input overload[2]	
50 Ω	|Peaks| ≤5 V, nominal
1 MΩ[3]	250 V_{rms}, nominal

Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet, for example, 115 V for U.S. or 230 V for Europe.

Caution Do not connect the PXIe-5164 to signals or use for measurements within Measurement Categories III or IV.

Accuracy

Caution The input terminals of this device are not protected for electromagnetic interference. As a result, this device may experience reduced measurement accuracy or other temporary performance degradation when connected cables are routed in an environment with electromagnetic interference. To limit the effects of this interference and to ensure that this device functions within specifications, take precautions when designing, selecting, and installing measurement probes and cables.

Resolution	14 bits
DC accuracy[4,5]	
50 Ω	±[(0.5% × |*Reading*|) + (0.2% of FS)]
1 MΩ	±[(0.65% × |*Reading* - *Vertical Offset*|) + (0.4% × |*Vertical Offset*|) + (0.2% of FS) + 0.15 mV]
DC drift[6]	±[(0.015% × |*Reading* - *Vertical Offset*|) + (0.001% × |*Vertical Offset*|) + (0.009% of FS)] per °C, nominal
AC amplitude accuracy[4]	±0.2 dB at 50 kHz

[2] Signals exceeding the maximum input overload may cause damage to the device.

[1] For input ranges between 2.5 V_{pk-pk} and 100 V_{pk-pk}, two offset ranges are possible. The driver software automatically picks the offset range that provides the highest resolution and accuracy.

Table 2. Crosstalk 50 Ω, Nominal[7]

Frequency	Level
1 MHz	-100 dB
10 MHz	-100 dB
100 MHz	-85 dB
400 MHz	-65 dB

Table 3. Crosstalk 1 MΩ, Nominal[7]

Frequency	Level	
	0.25 V_{pk-pk} to 10 V_{pk-pk}	**25 V_{pk-pk} to 100 V_{pk-pk}**
1 MHz	-85 dB	-70 dB
10 MHz	-85 dB	-70 dB
100 MHz	-75 dB	-55 dB
300 MHz	-60 dB	-40 dB

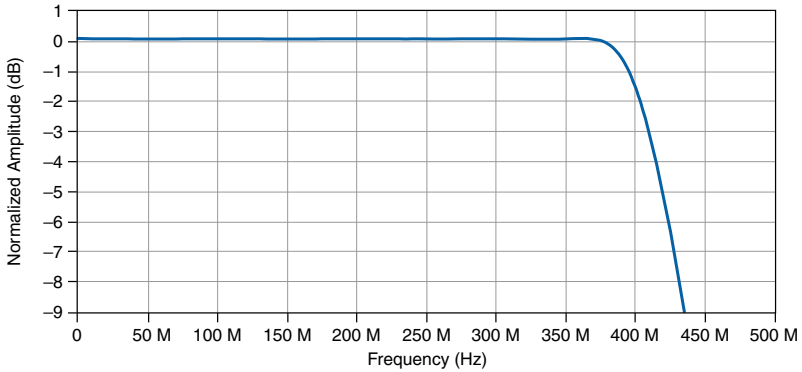
Bandwidth and Transient Response

Bandwidth (-3 dB)[10]	
50 Ω	400 MHz
1 MΩ[8]	300 MHz, nominal 285 MHz, warranted

[1] For input ranges between 2.5 V_{pk-pk} and 100 V_{pk-pk}, two offset ranges are possible. The driver software automatically picks the offset range that provides the highest resolution and accuracy.
[3] Derate above 500 kHz at 20 dB/dec until 5 MHz, then derate at 10 dB/dec.
[4] Within ± 5 °C of self-calibration temperature.
[5] Applies after averaging data for 8.5 ms
[6] Used to calculate errors when on board temperature changes more than ±5 °C from the self-calibration temperature.
[7] Measured on one channel with test signal applied to another channel, with the same range setting on both channels.
[8] Verified using a 50 Ω source and 50 Ω feedthrough terminator.

Bandwidth-limiting filters[10]	
Low-pass filters	20 MHz, nominal[9] 30 MHz, nominal[9] 150 MHz, nominal
High-pass filters[9]	90 Hz, nominal 450 Hz, nominal
Passband amplitude flatness[10]	
50 Ω	±0.5 dB from 50 kHz to 330 MHz
1 MΩ[8]	±0.7 dB from 50 kHz to 200 MHz
AC-coupling cutoff (-3 dB)[11]	
50 Ω	40 kHz, nominal
1 MΩ[8]	7.5 Hz, nominal
Rise/fall time[12]	
50 Ω	1 ns, nominal
1 MΩ[8]	1.5 ns, nominal

Figure 3. 50 Ω Full Bandwidth Frequency Response, 1 V_{pk-pk}, Nominal



9 Only available in NI-SCOPE.
10 Normalized to 50 kHz.
11 Verified using a 50 Ω source.
12 50% FS input pulse.

Figure 4. 50 Ω Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Nominal

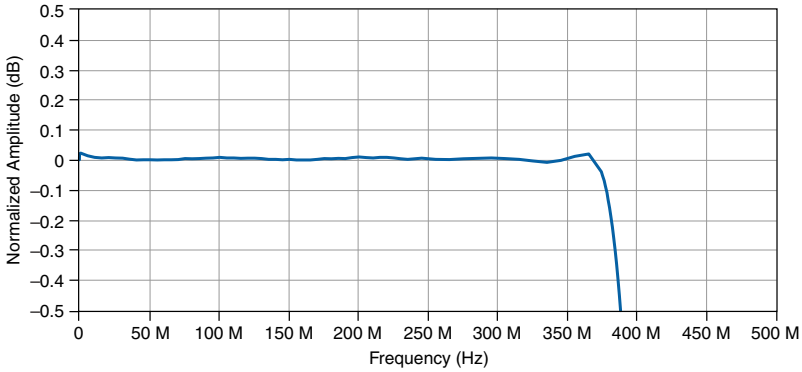


Figure 5. 50 Ω 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Nominal

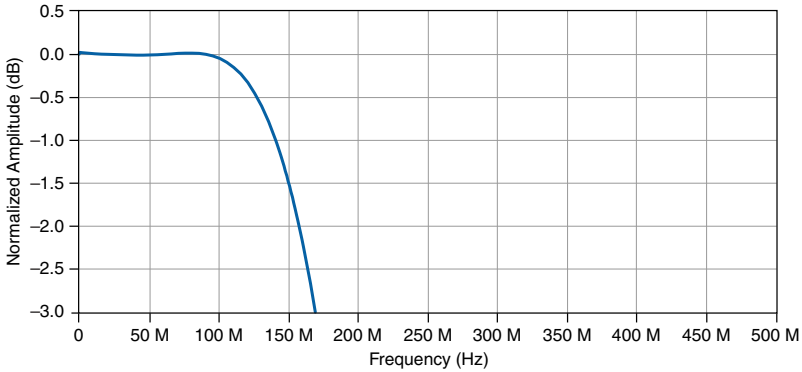


Figure 6. 1 MΩ Full Bandwidth Frequency Response, 1 V_{pk-pk}, Nominal

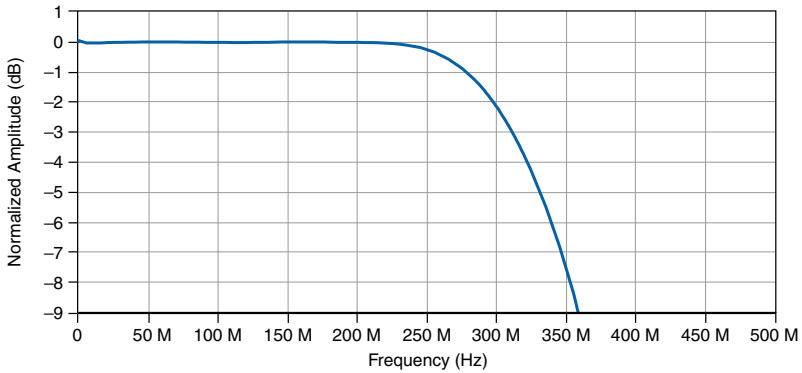


Figure 7. 1 MΩ Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Nominal

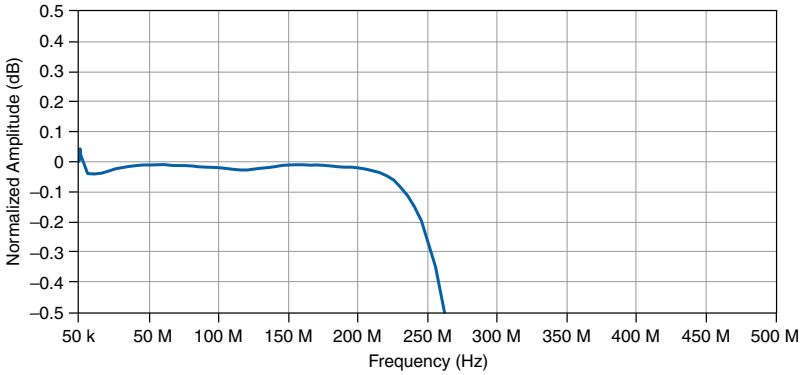
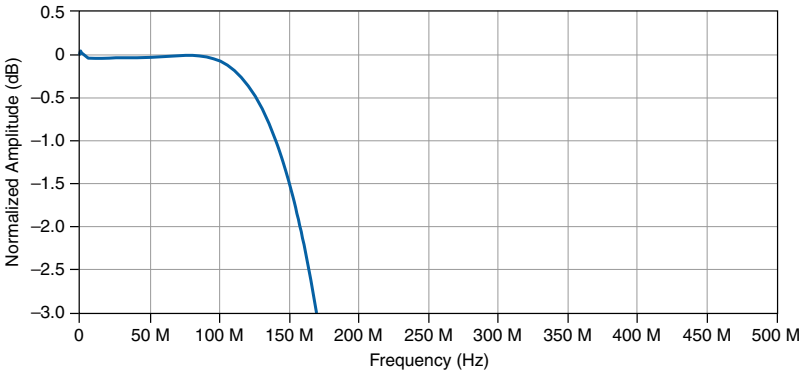


Figure 8. 1 MΩ 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Nominal



Spectral Characteristics

50 Ω Spectral Characteristics[16]

Table 4. Spurious-Free Dynamic Range (SFDR), Nominal[13]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <350 MHz, Full Bandwidth (dBc)
0.25 V	-70	-66
0.5 V	-73	-65
1 V	-74	-66

[13] -1 dBFS input signal corrected to FS. 1 kHz resolution bandwidth.

Table 4. Spurious-Free Dynamic Range (SFDR), Nominal[13] (Continued)

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <350 MHz, Full Bandwidth (dBc)
2.5 V	-71	-63
5 V	-69	-60

Table 5. Total Harmonic Distortion (THD), Nominal[14]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <350 MHz, Full Bandwidth (dBc)
0.25 V	-70	-62
0.5 V	-73	-61
1 V	-73	-62
2.5 V	-70	-62
5 V	-70	-60

Table 6. Effective Number of Bits (ENOB), Nominal[13]

Input Range (V_{pk-pk})	<350 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	9.4	10.7
0.5 V	9.5	10.9
1 V	9.5	11.0
2.5 V	9.6	11.1
5 V	9.5	11.0

[13] -1 dBFS input signal corrected to FS. 1 kHz resolution bandwidth.
[14] -1 dBFS input signal corrected to FS. Includes the second through the fifth harmonics.

1 MΩ Spectral Characteristics[15,16]

Table 7. Spurious-Free Dynamic Range (SFDR), Nominal[13]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)	>100 MHz to <250 MHz, Full Bandwidth (dBc)
0.25 V	-61	-57
0.5 V	-56	-50
1 V	-49	-43
2.5 V	-59	-55
5 V	-53	-47

Table 8. Total Harmonic Distortion (THD), Nominal[14]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	50 MHz to 250 MHz, Full Bandwidth (dBc)
0.25 V	-73	-58
0.5 V	-68	-50
1 V	-62	-43
2.5 V	-70	-56
5 V	-64	-48

Table 9. Effective Number of Bits (ENOB), Nominal[13]

Input Range (V_{pk-pk})	<250 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	8.8	9.6
0.5 V	8.1	9.8
1 V	7.0	9.0
2.5 V	8.6	9.5
5 V	7.7	9.5

[15] Verified using a 50 Ω source and 50 Ω feedthrough terminator.
[16] Excludes ADC Interleaving spurs.

Figure 9. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Nominal

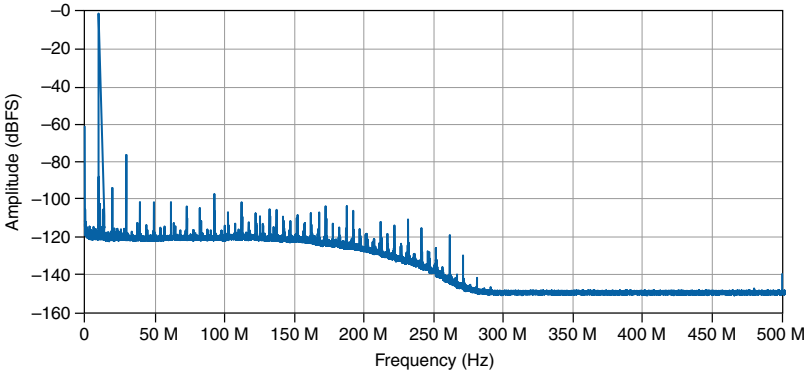


Figure 10. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Nominal

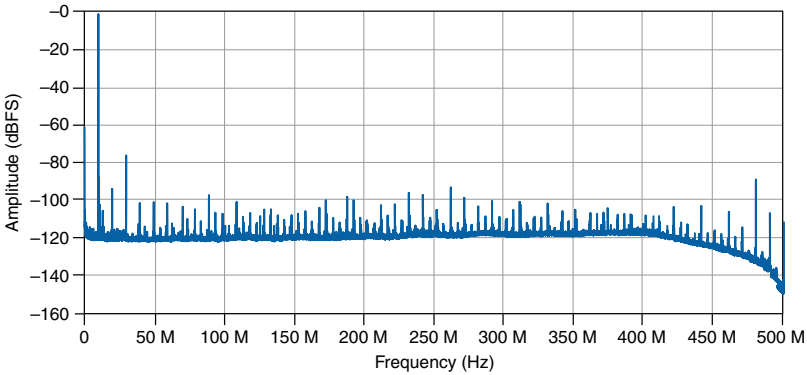


Figure 11. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 99.9 MHz Input Tone at -1 dBFS, Nominal

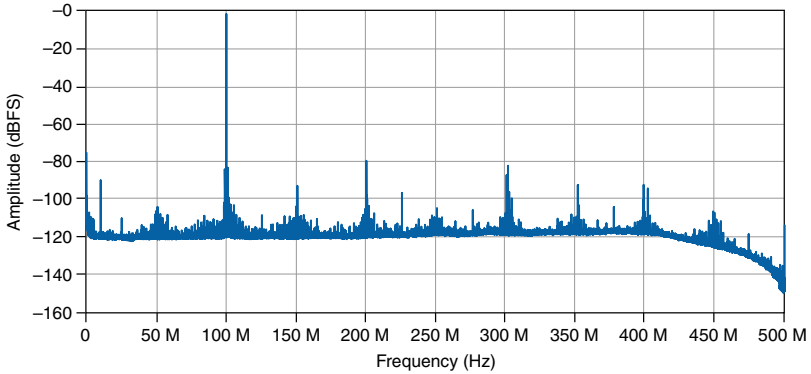


Figure 12. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Nominal

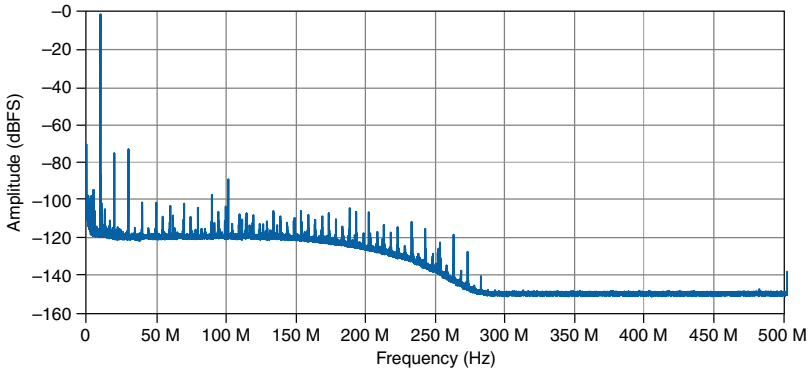
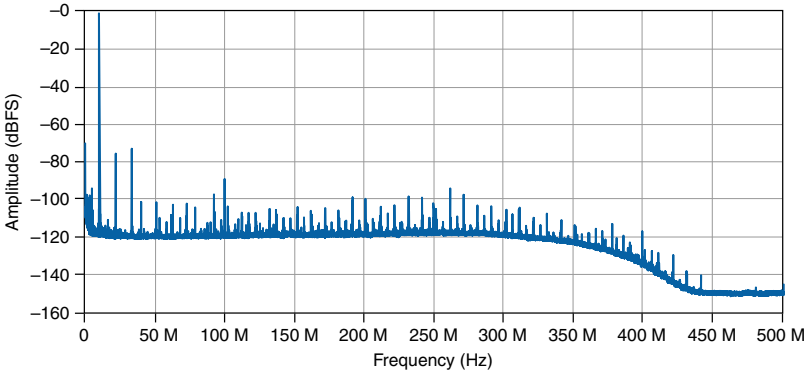


Figure 13. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Nominal



Noise[17]

50 Ω RMS Noise

Table 10. RMS Noise (Full Bandwidth)

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.045
0.5 V	0.040
1 V	0.035
2.5 V	0.030
5 V	0.030

Table 11. RMS Noise (150 MHz Filter), Typical

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.018
0.5 V	0.018
1 V	0.017
2.5 V	0.017
5 V	0.014

[17] Verified with 50 Ω terminator connected directly to BNC input.

Figure 14. 50 Ω Channel 0 Average Noise Density, 1 V_{pk-pk} Range, Nominal

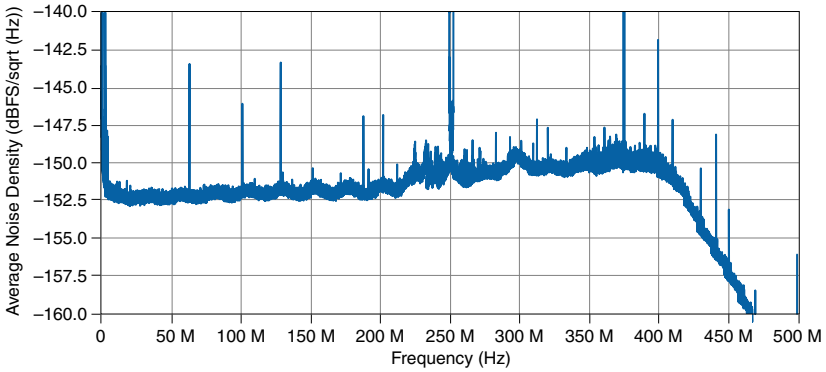
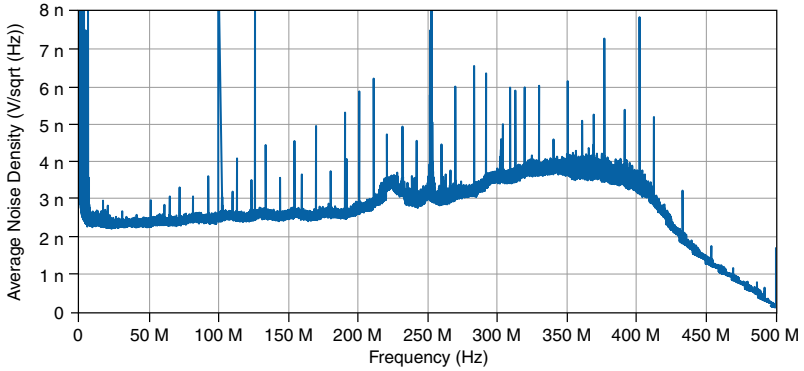


Figure 15. 50 Ω Channel 0 Average Noise Density, 0.25 V_{pk-pk} Range, Nominal



1 MΩ RMS Noise

Table 12. RMS Noise (Full Bandwidth)

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.110
0.5 V	0.060
1 V	0.050
2.5 V	0.100
5 V	0.060
10 V	0.050

Table 12. RMS Noise (Full Bandwidth) (Continued)

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
25 V	0.080
50 V	0.060
100 V	0.050

Table 13. RMS Noise (150 MHz Filter), Typical

Input Range (V_{pk-pk})	RMS Noise (% of Full Scale)
0.25 V	0.070
0.5 V	0.050
1 V	0.030
2.5 V	0.100
5 V	0.050
10 V	0.030
25 V	0.060
50 V	0.040
100 V	0.030

Skew

Channel-to-channel skew (full bandwidth)	
50 Ω	<100 ps, nominal
1 MΩ	<150 ps, nominal

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCTCXO)
External	CLK IN (front panel SMB connector) PXIe-DSTAR_A (backplane connector)

Sample rate range, real-time[18]	15.259 kS/s to 1 GS/s
Timebase frequency	1.0 GHz
Timebase accuracy	
Phase-locked to Onboard clock	±5 ppm
Phase-locked to External clock	Equal to the External clock accuracy
Sample clock jitter[19]	500 fs_{rms}, nominal

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal VCTCXO) PXI_CLK10 (backplane connector)
External (10 MHz)	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%, typical

External Sample Clock

Source	CLK IN (front panel SMB connector)
Impedance	50 Ω, nominal
Coupling	AC
Frequency	1.0 GHz
Input voltage range, when configured as a sample clock	632 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a sample clock	6 V_{pk-pk}, nominal
Duty cycle tolerance	45% to 55%, typical

External Reference Clock In

Sources	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Impedance	50 Ω, nominal

[18] Divide by *n* decimation from 1.0 GS/s used for all rates less than 1.0 GS/s. For more information about the Sample clock and decimation, refer to the *NI High-Speed Digitizers Help*.

[19] Integrated from 100 Hz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

Coupling	AC
Frequency[20]	10 MHz
Input voltage range, when configured as a Reference clock	623 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a Reference clock	6 V_{pk-pk}, nominal

Reference Clock Out

Source	PXI_CLK10 (backplane connector)
Destination	AUX 0 CLK OUT (front panel MHDMR connector)
Output impedance	50 Ω, nominal
Logic type	3.3 V CMOS
Maximum current drive	±12 mA, nominal

Trigger

Note The following characteristic behaviors are valid when using the device with NI-SCOPE API. When using instrument design libraries, these characteristics may not be valid.

Supported triggers	Reference (stop) trigger Reference (arm) trigger Start trigger Advance trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 CH 1 SMB PFI 0 AUX 0 PFI <0..7> PXI_Trig <0..6> Software

[20] The PLL Reference clock must be accurate to ±25 ppm.

Dead time	40 ns
Trigger delay	from 0 ns to 2.25×10^{15} ns ((2^{51}-1)*`Sample clock period` ns)
Rearm time	496 ns
Hold off	From dead time to 1.84×10^{19} ns ((2^{64} - 1)*`Sample clock period` ns)

Analog Trigger

Sources	CH 0 CH 1
Time resolution with interpolator[21]	`Sample clock period`/1024 = 0.977 ps
Time resolution without interpolator	Sample clock period (1 ns)
Trigger filters	
Low Frequency (LF) Reject	100 kHz
High Frequency (HF) Reject	100 kHz
Trigger accuracy[22]	0.5% of full scale, nominal
Trigger jitter[22]	15 ps_{rms}, nominal
Minimum threshold duration[23]	Sample clock period

Digital Trigger

Sources	PFI 0 (front panel SMB connector) AUX 0 PFI <0..7> (front panel MHDMR connector) PXI_Trig <0..6> (backplane connector)
Time resolution	8 ns

21 Requires NI-SCOPE.

22 Analog triggers. For input frequencies less than 250 MHz.

23 Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

Programmable Function Interface

Connectors	AUX 0 PFI <0..7> (front panel MHDMR connector) PFI 0 (front panel SMB connector)
Direction	Bidirectional per channel
Direction control latency	125 ns
As an Input (Trigger)	
Destination	FPGA diagram Start trigger (acquisition arm) Reference (stop) trigger Arm Reference Trigger Advance trigger
Input impedance	49.9 kΩ, nominal
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	3.3 V nominal
Maximum input overload	0 to 3.3 V nominal 5 V tolerant
Maximum frequency	50 MHz
Minimum pulse width	10 ns
As an Output (Event)	
Sources	FGPA diagram Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe Compensation[24]
Output impedance	50 Ω, nominal
Logic type	3.3 V CMOS
Maximum current drive	12 mA, nominal

[24] 1 kHz, 50% duty cycle square wave, SMB PFI 0 only.

Maximum frequency	50 MHz
Minimum pulse width	10 ns

AUX 0 Connector Specifications

Connector	MHDMR
Voltage output	3.3 V ± 10%, nominal
Maximum current drive on +3.3 V	200 mA, nominal
Output impedance on +3.3 V	<1 Ω, nominal

Waveform Specifications

Onboard memory size[25]	1.5 GB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (record length - 1)
Number of posttrigger samples	Zero up to record length
Maximum number of records in onboard memory[26]	4,194,304 for 1.5 GB

Table 14. Examples of Allocated Onboard Memory Per Record (1.5 GB Onboard Memory)

Channels	Bytes Per Sample	Max Records Per Channel	Record Length	Allocated Onboard Memory Per Record
1	2	4,194,304	1	384
1	2	671,088	1,000	2,400
1	2	79,137	10,000	20,352
1	2	1	805,306,192	1,610,612,736
2	2	4,194,304	1	384
2	2	364,722	1,000	4,416

[25] Onboard memory is shared among all enabled channels.

[26] You can exceed these numbers if you fetch records while acquiring data. For more information, refer to the *NI High-Speed Digitizers Help*.

Table 14. Examples of Allocated Onboard Memory Per Record (1.5 GB Onboard Memory) (Continued)

Channels	Bytes Per Sample	Max Records Per Channel	Record Length	Allocated Onboard Memory Per Record
2	2	39,850	10,000	33,216
2	2	1	402,653,096	1,610,612,736

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at *ni.com/manuals*.

FPGA

FPGA model	Xilinx Kintex-7 XC7K410T FPGA
Xilinx Kintex-7 XC7K410T FPGA Resources	
Slice registers	508,400
Slice look-up tables (LUT)	254,200
DSPs	1,540
18 Kb block RAMs	1,590

Note Note that some of these resources are consumed by the logic necessary to operate the device and integrate with software, and are thus out of the control of users.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.
- Corrects the frequency response for all ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Interleaving spurs
- Intermodule synchronization errors

Refer to the *NI High-Speed Digitizers Help* for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[27]	15 minutes

Software

Driver Software

This device was first supported in NI-SCOPE 16.1 and NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes 16.1. NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes is an IVI-compliant driver that allows you to configure, control, and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

Related Information

For more information about available software options, refer to the PXIe-5164 Getting Started Guide.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio

[27] Warm-up begins after the chassis and controller or PC is powered. In some RIO applications, the power consumed by the module can be significantly higher than the default image for the module. In these cases, you can improve performance by loading your image and configuring the device before warm-up time begins. Self-calibration is recommended following the specified warm-up time.

- Microsoft Visual C/C++
- .NET (C# and VB.NET)

LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes allows the use of the LabVIEW FPGA Module to customize the device FPGA to create application-specific instrument designs.

Interactive Soft Front Panel and Configuration

The NI-SCOPE Soft Front Panel (SFP) allows interactive control of the PXIe-5164.

Interactive control of the PXIe-5164 was first available in NI-SCOPE SFP version 16.1. The NI-SCOPE SFP is included on the NI-SCOPE media.

NI Measurement Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5164. MAX is included on the NI-SCOPE and NI LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at *ni.com/support*.

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each module.
- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.

Note Although you can use NI-TClk to synchronize non-identical SMC-based modules, these specifications apply only to synchronizing identical modules.

Skew[28]	300 ps, nominal
Skew after manual adjustment	≤10 ps, nominal
Sample clock delay/adjustment resolution	3.5 ps

[28] Caused by clock and analog delay differences. No manual adjustment performed. Tested with a PXIe-1082 chassis with maximum slot to slot skew of 100 ps. Valid within ±1 °C of self-calibration.

Bus Interface

Form factor	PXI Express (x8 Gen 2)
Slot compatibility	PXI Express or hybrid
DMA channels	32

Power

+3.3 VDC	6.5 W, typical
+12 VDC	18.5 W, typical
Total power	25 W, typical
Total maximum power allowed	38.25 W, typical

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 module 21.26 cm × 12.88 cm × 2.0 cm (8.37 in × 5.07 in × 0.787 in)
Weight	460 g (16.2 oz)

Environment

Maximum altitude	4,600 m (570 mbar) (at 25 °C ambient temperature)
Measurement category	II
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 50 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61000-6-1 (IEC 61000-6-1): Immunity
- EN 61000-6-3 (IEC 61000-6-3): Class A emissions
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity

- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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